WHAT IS CLAIMED IS:

1. A computer which processes an interrupt when an instruction in a program is executed, said computer comprising:

a data holding part which holds data at a time when said interrupt starts to occur.

2. The computer as claimed in claim 1, wherein said data holding part includes a plurality of registers.

3. The computer as claimed in claim 2, said computer further comprising flags each of said flags indicating whether said data is held in said register.

4. The computer as claimed in claim 1, said computer further comprising a data storing part, wherein said data holding part holds said data to be stored in said data storing part at a time when said interrupt occurs while a store instruction is executed, said store instruction requesting that said data is stored in said data storing part.

5. The computer as claimed in claim 1, wherein said data holding part holds an instruction address of an instruction which causes said interrupt.

6. The computer as claimed in claim 1, wherein said data holding part holds data which indicates a factor of said interrupt.

7. The computer as claimed in claim 1, wherein said data holding part holds an effective address of a load instruction or a store instruction when said interrupt occurs while said load instruction or said store instruction is executed.

8. The computer as claimed in claim 1, wherein said data is used for recovery from said interrupt.

9. A control method of a computer which processes an interrupt when an instruction in a program is executed, said method comprising the step of:

holding data at a time when said interrupt starts to occur.

10. The control method as claimed in claim 9, wherein said data is held in a plurality of registers and said data is used for recovery from a plurality of interrupts.

11. The control method as claimed in claim 10, wherein flags are used in which each of which flags indicates whether said data is held in said register.

12. The control method as claimed in claim 9, said control method comprising the step of:

holding said data to be stored in a data storing part in said computer at a time when said interrupt occurs while a store instruction is executed, said store instruction requesting that said data is stored in said data storing part.

13. The control method as claimed in claim 9, said control method comprising the step of:

holding an instruction address of an instruction which causes said interrupt.

14. The control method as claimed in claim 9, said control method comprising the step of:

holding data which indicates a factor of said interrupt.

15. The control method as claimed in claim 9, said control method comprising the step of:

holding an effective address of a load instruction or a store instruction when said interrupt occurs while said load instruction or said store instruction is executed.

16. The control method as claimed in claim 9, wherein said data is used for recovery from said interrupt.